

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet

1

of

Complete if Known

Application Number	10/601,351
Filing Date	June 23, 2003
First Named Inventor	Crafts, Harold S.
Art Unit	2812
Examiner Name	
Attorney Docket Number	000939-052170US

U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No. ¹	Document Number Number Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
DA	AA	US-2002/0153574 A1	10/24/2002	Crafts	
	AB	US-			
	AC	US-			
	AD	US-			
	AE	US-			
	AF	US-			
	AG	US-			
	AH	US-			
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	AP	US-			
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FOREIGN PATENT DOCUMENTS

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Sheet **2** of**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
OW	BC	CHANG, M. & CHEN, C. "PROMPT3 - A Cell-Based Transistor Sizing Program Using Heuristic and Simulated Annealing Algorithms." IEEE, 1989, pp. 17.2.1-17.2.4.	
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		Number	Kind Code ² (if known)			
OH	AA	US-4,742,383		05/03/1988	Fitzgerald	
DA	AB	US-5,410,173		04/25/1995	Kikushima et. al	
	AC	US-				
	AD	US-				
	AE	US-				
	AF	US-				
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	AZ							<input type="checkbox"/>
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U.S. PATENT DOCUMENTS

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		Number	Kind Code ² (if known)			
001	AA	US-5,342,794		08/1994	Wei, Yi-Hen	
	AB	US-5,286,518		02/1994	Cain, et al.	
	AC	US-3,481,381		08/01/1969	Delivorias	
	AD	US-4,151,635		05/1979	Kashkooli et al.	
	AE	US-4,143,178		05/01/1979	Harada et al.	
	AF	US-4,229,756		10/21/1980	Sata et al.	
	AG	US-4,244,001		01/06/1981	Alfred C. Ipri	
	AH	US-4,317,690		03/02/1982	Koomen et al.	
	AI	US-4,525,809		08/25/1985	Chiba et al.	
	AJ	US-4,584,653		04/22/1986	Chih et al.	
	AK	US-4,593,205		08/03/1986	Bass et al.	
	AL	US-4,630,219		12/16/1986	DiGiacomo et a	
	AM	US-4,638,458		01/20/1987	Itoh	
	AN	US-4,682,202		07/21/1987	Tanizawa	
	AO	US-4,686,758		08/18/1987	Liu et al.	
	AP	US-4,701,642		10/20/1987	Pricer	
	AQ	US-4,845,544		07/04/1989	Shimizu	
	AR	US-4,849,344		07/18/1989	Desbiens et al.	
	AS	US-4,905,073		02/27/1990	Chen et al.	
	AT	US-4,989,062		01/29/1991	Takahashi et al.	
	AU	US-4,999,518		03/12/1991	Dhong et al.	
	AV	US-5,003,199		03/26/1991	Chuang et al.	
	AW	US-5,008,208		04/04/1991	Liu et al.	
	AX	US-5,013,679		05/07/1991	Kumagai et al.	
	AY	US-5,032,530		07/16/1991	Lowrey et al.	
	AZ	US-5,037,766		08/06/1991	Wang	
	BA	US-5,045,726		09/03/1991	Leung	
	BB	US-5,049,515		09/17/1991	Tzeng	
	BC	US-5,081,518		01/14/1992	El-Dwany et al.	
	BD	US-5,124,776		06/23/1992	Tanizawa et al.	
	BE	US-5,126,279		06/30/1992	Roberts	
	BF	US-5,162,884		11/10/1992	Liou et al.	
	BG	US-5,168,072		12/01/1992	Moslehi	

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DA	BH	US-5,175,118	12/29/1992	Yoneda	
	BI	US-5,225,991	07/06/1993	Dougherty	
	BJ	US-5,294,822	03/15/1994	Verrett	
	BK	US-5,296,755	03/22/1994	Miyamoto et al.	
	BL	US-5,298,805	03/29/1994	Garverick et al.	
	BM	US-5,313,079	05/17/1994	Brasen et al.	
	BN	US-5,313,101	05/17/1994	Harada et al.	
	BO	US-5,314,832	05/24/1994	Deleonibus	
	BP	US-5,341,049	08/23/1994	Shimizu et al.	
	BQ	US-5,388,055	02/07/1995	Tanizawa et al.	
	BR	US-5,432,707	07/11/1995	Leung	
	BS	US-5,444,285	08/22/1995	Robinson et al.	
	BT	US-5,452,245	09/19/1995	Hickman et al.	
	BU	US-5,539,224	07/01/1996	Ema	
	BV	US-5,541,120	07/30/1996	Robinson et al.	
	BW	US-5,654,898	08/05/1997	Roetscender et al.	
	BX	US-5,671,397	09/23/1997	Crafts	
DA	BY	US-5,869,900	02/09/1999	Crafts	
	BZ	US-6,269,466	07/31/2001	Crafts	

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DA	CA	IBM Technical Disclosure Bulletin; Vol. 25, No. 4; September 1982; Structured Macro; E.H. STOOPS	
	CB	An Efficient Algorithm for some Mltirow Layout Problems; J. FELDMAN et al.; IEEE Transactions on Computer-Aided Design of Integrated Circuits & Systems; Vol. 12, No. 8, August 1993; pp. 1178-1185	
	AC	10K-Gate GaAs JFET Sea of Gates; H. KAWASAKI et al.; IEEE Journal of Solid-State Circuits; vol. 26, No. 10; October 1991; pp. 1367-1370	
	AD	A Comprehensive CAD System for High-Performance 300K-Circuit ASIC Logic Chips; J. PANNER et al.; IEEE Journal of Solid-State Circuits; vol. 26, No. 3; March 1991; pp. 300-309	
	AE	A Design-System for ASIC's with Macrocells; B. KORTE et al.; IEEE, Euro ASIC '90; 1990; PP. 220-224	
	AG	GaAs MESFET and SiCMOS Cointegration & Circuit Techniques; H. SHICHIJO et al.; IEEE, GaAs IC Symposium, September 1988; pp. 239-242	
	AG	Application of AlGaAs/GaAs HBT's to High-Speed CML Logic Family Fabrication; M. MADIHAN et al.; IEEE Transactions on Electron Devices, Vol. 36, No. 4, April 1989; pp. 625-631	
	AH	Combining Partitioning and Global Routing in a Sea-of-Cells Design; B. KORTE et al., IEEE Computer-Aided Design; 1989 International Conference; pp. 98-101	
	AI	Size Optimization for CMOS Basic Cells of VLSI, IEEE, pp. 2180-2183, HSIEH et al.	
	AJ	Dependence of Spice level 3 Model Parameters with tRansistor Size, IEEE, pp. 84-89, PERELLO et al.	
	AK	BACHELU et al. "A Study of the Use of Local Interconnect in CMOS Leaf Cell Design," IEEE, pp. 566-570, 1993	
	AL	BACHELU et al. "A Study of the Use of Local Interconnect in CMOS Leaf Cell Design," IEEE, pp. 1258-1261, 1992	
DA	AM	BARTELINK et al. "Interconnect for Submicron ASICs," IEEE, pp. 59-62, 1989	

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